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EXAMINER	
YANG, HAN	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
06/12/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 03/24/2006, are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. This action is responsive to the amendment on 02/04/2008 **Claims 1-12** are pending. **Claims 1** have been amended; **claim 6** has been canceled, and **claims 11-12** has been added.

3. Applicant's arguments, see Remarks, filed 12/14/2005, with respect to the drawing have been fully considered and are persuasive.

4. Applicant's argument filed on 02/04/2008 with respect to **claims 1-5, 7-12** have been fully considered but they are persuasive, a new ground(s) of rejection are introduced.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. **Claims 1-5, 7-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Keshtbod** (US Patent 4,527,255) in view of **Lee** (US Patent 7,164,608 B2).

7. ***Regarding Independent claim 1***, Keshtbod teaches a static memory (**Fig. 2, Q1, Q2**) defining at least first and second nodes (**Fig. 2, N1, N2**) communicatively connected with read and/or write data lines (**Fig. 2, #23, #24**);

at least one non-volatile memory (**Fig. 2, Q3, Q4**) associated with the static memory (**Fig. 2, Q1, Q2**), and writing data stored therein to the static memory (**Fig. 2, Q1, Q2**);

the non-volatile memory (**Fig. 2, Q3, Q4**) comprising a first non-volatile element (**Fig. 2, Q3**) having a control gate connected to a first node (**Fig. 2, N2**) and a source connected to a second node (**Fig. 2, N1**), and a second non-volatile element (**Fig. 2, Q4**) having a control gate connected to the second node (**Fig. 2, N1**) and a source connected to the first node (**Fig. 2 N2**), the drain of each non-volatile element (**Fig. 2, Q3, Q4**) being connected by of a respective transistor (**Fig. 2, Q5, Q6**) to a supply voltage;

characterized in that the respective transistors (**Fig. 2, Q5, Q6**) are arranged to isolate

the drains (**Fig. 2 D3, D4**) of the first and second non-volatile elements from the supply during a program cycle of the memory device (**Fig. 2, #30**).

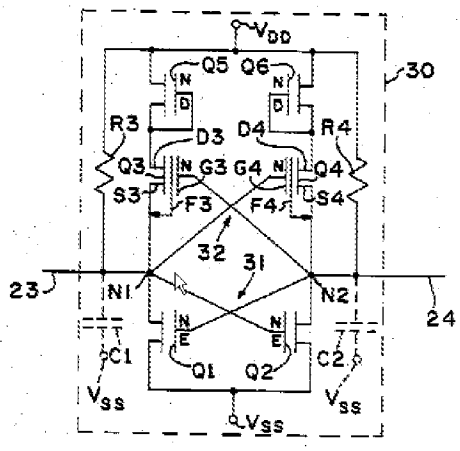

Fig. 2

Keshtbod is silent with respect to the static memory means comprises a pair of cross-coupled inverters.

Lee teaches the static memory (**Fig. 9, #406, #407**) means comprises a pair of cross-coupled inverters (**Fig. 9, #470, #472**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of **Lee** to the teaching of **Keshtbod** such that the reading process of six transistors SRAM cells is easier than four transistors SRAM cells.

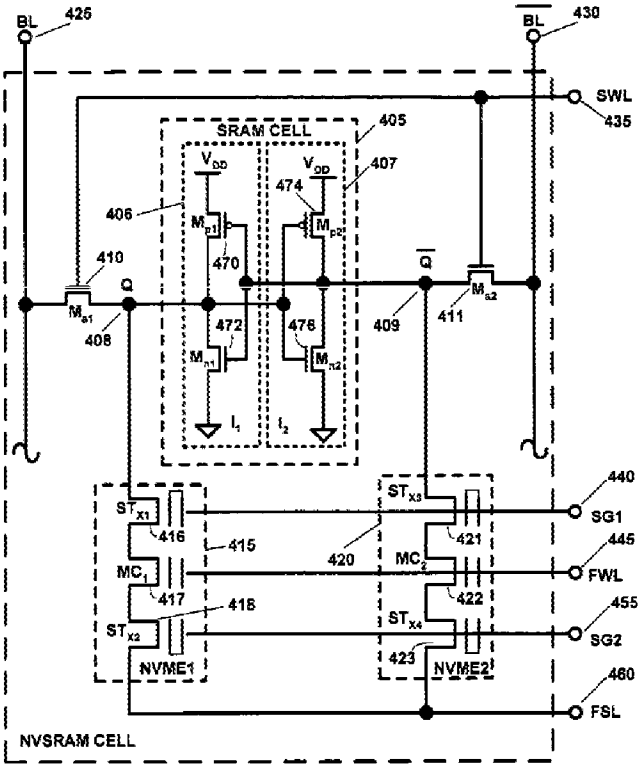

Fig. 9

8. ***Regarding claim 2***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise embedded flash or EEPROM elements (**Abstract, lines 3-5**).

9. ***Regarding claim 3***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise double or single poly floating gate type memory cells (**Abstract, lines 3-5**).

10. ***Regarding claim 4***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise devices, which can be programmed and erased by of tunneling of charges (**column 4, lines 58-61**).

11. ***Regarding claim 5***, Keshtbod teaches the non-volatile memory elements (**Fig. 2,**

Q3, Q4) are programmed with opposite data (**column 7 lines 1-3, 13-15**).

12. ***Regarding claim 7***, Keshtbod teaches one or more respective selection transistors (**Fig. 1, Q7, Q8**) are provided, by of which the nodes (**Fig. 1, Fig. 2, #23, #24**) are communicatively coupled to the read and/or write lines (**Fig. 1**).

13. ***Regarding claim 8***, Keshtbod teaches respective selection transistors (**Fig. 1, Q7, Q8**) are including one or more isolation transistors (**Fig. 1, Q7, Q8**).

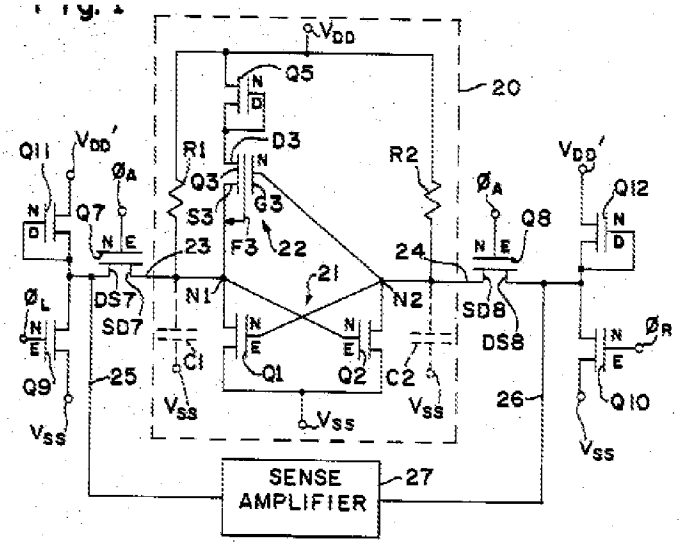

Fig. 1

14. ***Regarding claim 9***, Keshtbod teaches reconfigurable programmable logic device (**Fig. 4, column 10, lines 8-16**).

15. ***Regarding claim 9***, Keshtbod teaches a field programmable gate array including a memory device (**Fig. 4, column 10, lines 8-16**).

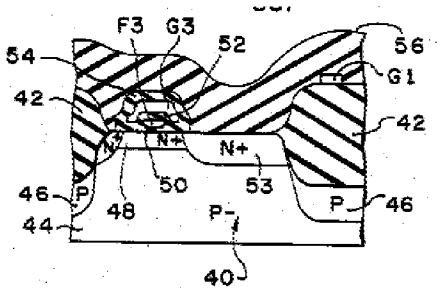

Fig. 4

16. ***Regarding claim 11,*** Keshtbod teaches all of the limitation s discussed above (from which these claims depend).

Keshtob is silent with respect to gates of the respective transistors are connected together to receive a common signal.

Lee teaches gates of the respective transistors are connected together to receive a common signal (**Fig. 9, #440**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of **Lee** to the teaching of **Keshtob** such that it's easy to control nonvolatile memory cells with common wordline.

17. ***Regarding claim 12***, Keshtbod teaches all of the limitation s discussed above (from which these claims depend).

Keshtbod is silent with respect to each of the cross-coupled inverters includes a pair of transistors, gates of the transistors of a first inverter of the cross-coupled inverters being connected to the second non-volatile element, gates of the transistors of a second inverter of the cross-coupled inverters being connected to the first non-volatile element.

Lee teaches each of the cross-coupled inverters (**Fig. 9, #406, #407**) includes a pair of transistors (**Fig. 7, #470, 472**), gates of the transistors of a first inverter of the cross-coupled inverters being connected to the second non-volatile element (**Fig. 9, gate of M_{p1} and M_{n1} connect to #421**), gates of the transistors of a second inverter of the cross-coupled inverters being connected to the first non-volatile element (**Fig. 9, gate of M_{p2} and M_{n2} connect to #416**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Lee to the teaching of Keshtbod such that the reading process of six transistors SRAM cells is easier than four transistors SRAM cells.

Response to Amendment

18. Applicant's arguments with respect to claim 1 has been considered but are moot in view of the new ground(s) of rejection, necessitated by amendment. See the rejection above.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Han Yang whose telephone is (571) 270-3048. The examiner can normally be reached on Monday-Friday 8am-5pm with alternate Friday off.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869 the fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

HY
03/10/2008
/Richard Elms/

Supervisory Patent Examiner, Art Unit 2824
3.17.08 & 5.6.08